



CQM4531-L-224-2

2x2 Wi-Fi + BLE5.4 IoT Hub Module

Catalogs

| | | |
|----------|--|-----------|
| 1 | <i>Product Overview</i> | 4 |
| 2 | <i>Hardware Specification</i> | 6 |
| 2.1. | Block Diagram | 6 |
| 2.2. | Pinout Description | 7 |
| 2.2.1. | Pin Map | 7 |
| 2.2.2. | Pin Definition | 8 |
| 2.3. | Computing Subsystem | 11 |
| 2.3.1. | SoC | 11 |
| 2.4. | Memory | 12 |
| 2.5. | Peripheral Interfaces | 12 |
| 3 | <i>Electrical Characteristics</i> | 14 |
| 3.1. | Absolute Maximum Ratings | 14 |
| 3.2. | Recommended Operating Conditions | 14 |
| 4 | <i>Radio Performance</i> | 15 |
| 4.1. | 2.4GHz Wi-Fi | 15 |
| 4.2. | Bluetooth | 15 |
| 5 | <i>Power Consumption</i> | 17 |
| 6 | <i>Mechanical Specification</i> | 18 |
| 6.1. | Dimension | 18 |
| 6.2. | Recommended PCB Landing Pattern | 19 |
| 7 | <i>Manufacturing Recommendation</i> | 20 |
| 7.1. | Power Layout Guideline | 20 |
| 7.2. | PCIe Layout Guideline | 20 |
| 7.3. | Ethernet Layout Guideline | 21 |
| 7.4. | USB Layout Guideline | 21 |

7.5. Soldering Recommendations.....22

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

1 Product Overview

Powered by Qualcomm QCA4531 and QCC711, CQM4531-L-224-2 is a purposely-designed soldered-down form factor BLE and Wi-Fi module that combine multi-core processing capabilities and high-security features to meet the demands of diverse IoT applications. Their compact size contributes to cost reduction, making them an attractive choice for space-constrained IoT edge devices.

The CQM4531-L-224-2 is based on the QCA4531 chipset, utilizing a MIPS 24Kc processor with a main frequency of 650MHz. The module supports 1Gbit DDR2, 1Gbit NAND SPI flash, and 4Mbit NOR flash. Additionally, the module offers a variety of interfaces, including PCIe, UART, USB 2.0, GPIO, SPI, IEEE 802.3 Fast Ethernet interface, and K.FL2 interface. The top wireless speed of CQM4531-L-224-2 reaches as high as 144Mbps at 20MHz and 300Mbps at 40MHz. Furthermore, CQM4531-L-224-2 also supports Bluetooth 5.4, ensuring seamless interoperability with other Bluetooth devices. As a result, CQM4531-L-224-2 can function as a Wi-Fi AP, a Wi-Fi client, or a Bluetooth device, making it widely useful in various IoT scenarios.

The CQM4531-L-224-2 runs on the open-source Linux operating system and the OpenWrt networking stack, simplifying software development for customers. The module has a communication stack that includes HTTP, IPv4, TCP, SSL, DHCP, ICMP, IGMP, and DNS. CQM4531-L-224-2 can function as an IoT Wi-Fi access point, with power optimization to suit low-power use cases.

CQM4531-L-224-2 includes the following configurations in the table:

| Module | Form Factor |
|-----------------|---|
| CQM4531-L-224-2 | 34.83 x 34.83 x 2.4 mm, 1.27 mm pitch, 104-pin, LGA |

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|------------------|----------|----------------|---------|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

CQM4531-L-224-2 module is graphically illustrated below:

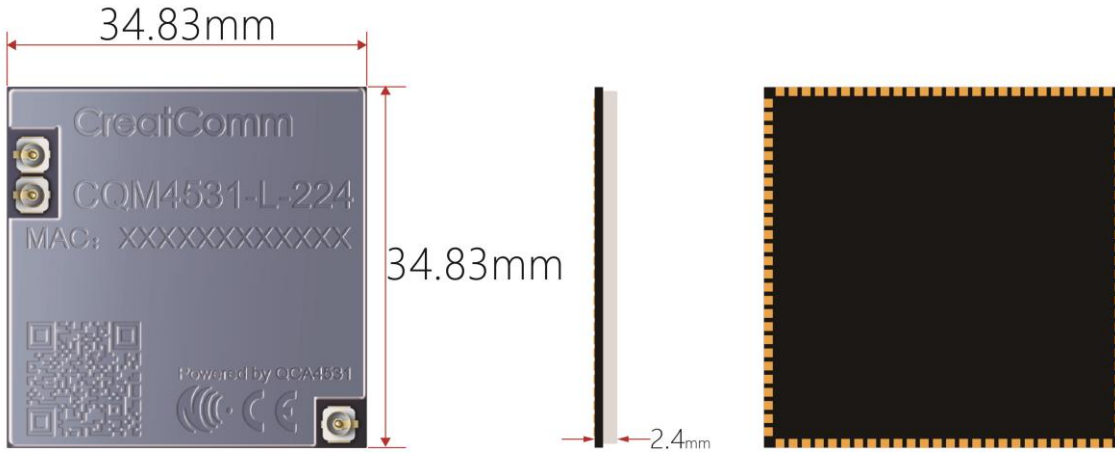


Figure 1: CQM4531-L-224-2 Module View

Development kits specific to the module are also provided to customers, facilitating the development of application software, as illustrated below.

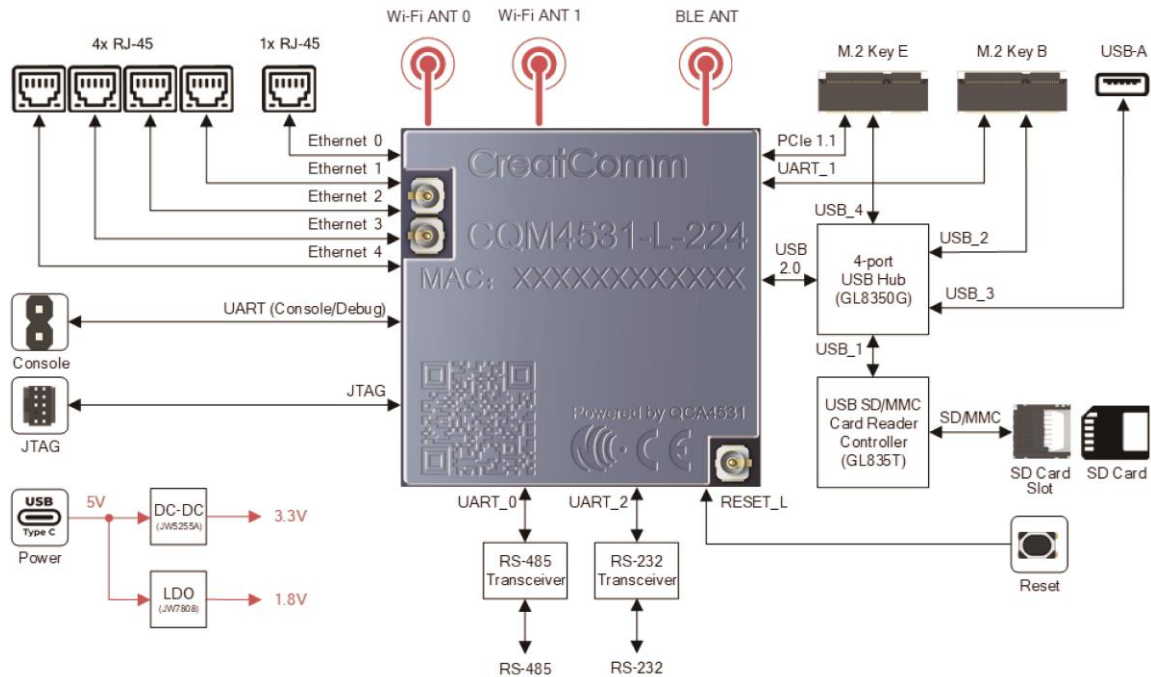


Figure 2: CQM4531-L-224-2 Development Kit block diagram

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|------------------|----------|----------------|---------|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

2 Hardware Specification

This section provides detailed hardware design and specifications of CQM4531-L-224-2.

2.1. Block Diagram

The CQM4531-L-224-2 supports multiple interfaces, including PCIe, UART, USB 2.0, GPIO, SPI, 5 IEEE 802.3 fast Ethernet interfaces, 2 K.FL2 (Wi-Fi), and 1 K.FL2 (Bluetooth).

The block diagram of the module is shown below.

QCA4531+QCC711 LGA/Header Module

2x2 2.4GHz Wi-Fi 4 + BLE 5.4 IoT Hub Module

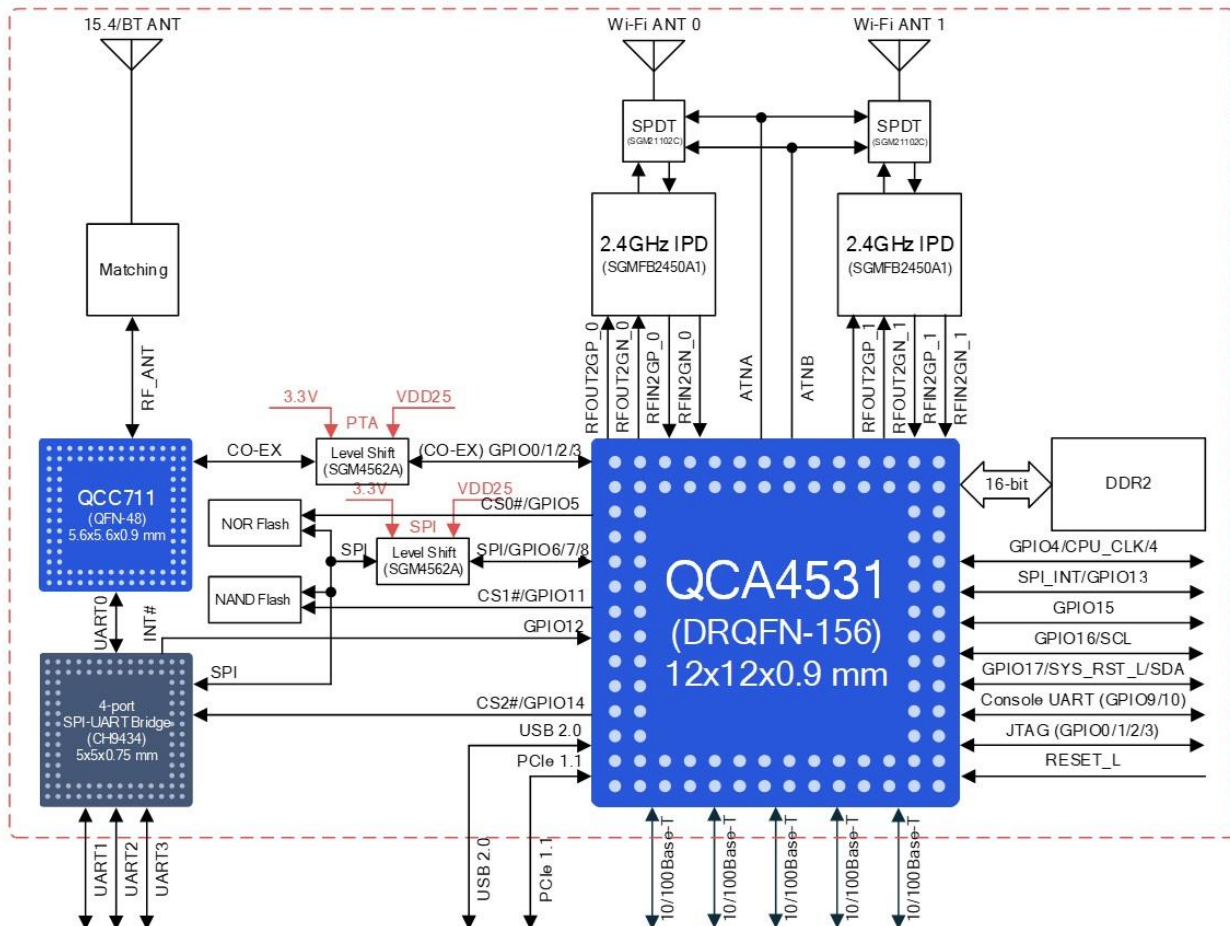


Figure 3: CQM4531-L-224-2 Block Diagram

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

2.2. Pinout Description

2.2.1. Pin Map

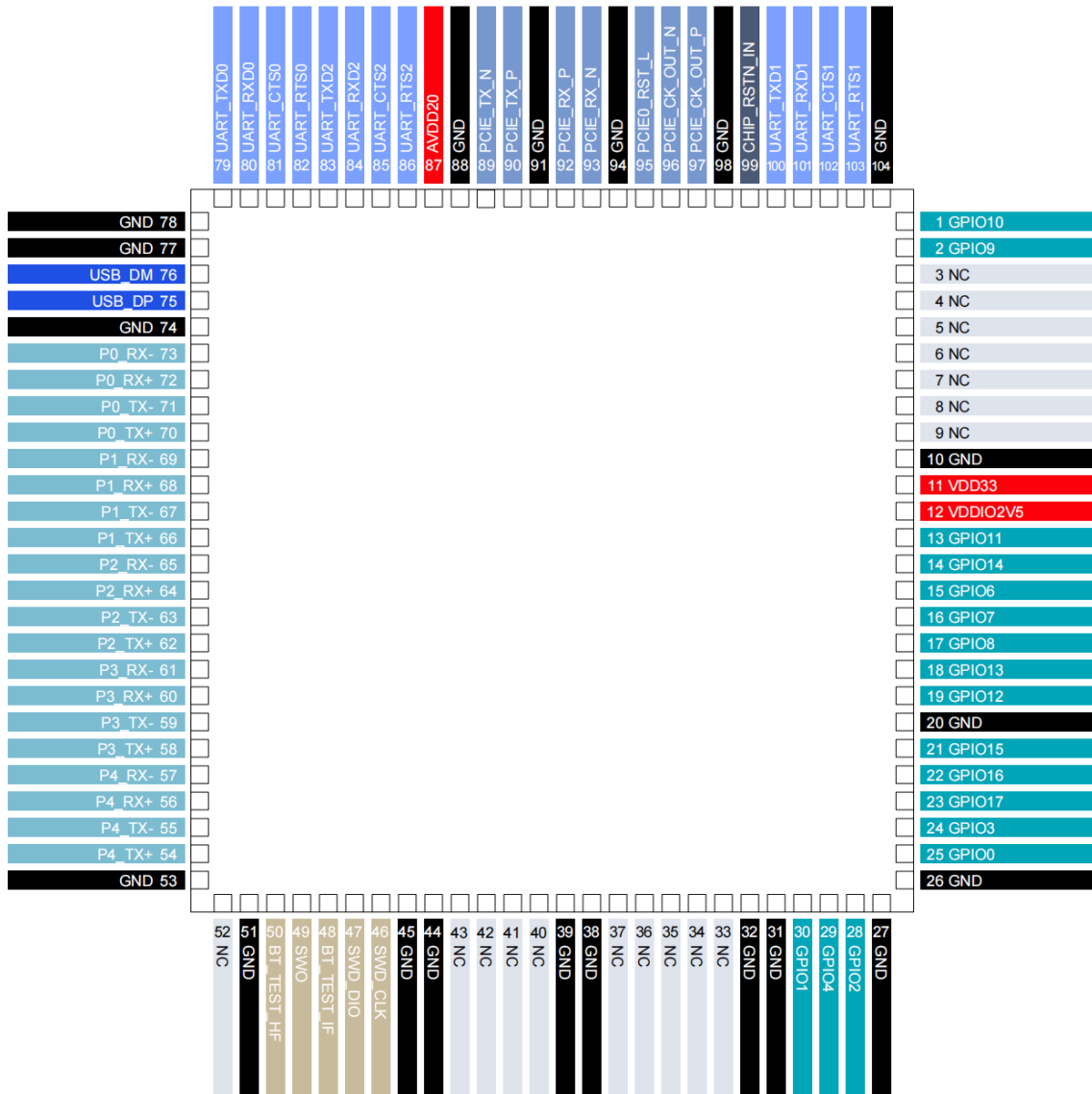


Figure 4: CQM4531-L-224-2 Pin Map

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

2.2.2. Pin Definition

| Pin | Pin Name | Domain | Type | Description |
|--|-------------------|----------|-------|---|
| 10,20,26 ,27,31,3 2,38,39, 44,45,51 ,53,74,7 7,78,88, 91,94,98 ,104 | GND | - | GND | Ground |
| 11 | VDD3V3 | - | IN | Power input (typical 3.3V) |
| 12 | VDDIO2V5 | - | OUT | QCA4531 I/O voltage (2.49~2.75V) |
| 87 | AVDD20 | - | OUT | Ethernet PHY (typical 2.0V) |
| 13 | GPIO11/SPI_CS1 | VDDIO2V5 | DI/DO | Default for SPI nand chip select (Reserved) |
| 14 | GPIO14/SPI_CS2 | VDDIO2V5 | DI/DO | Default for CH9434 chip select (Reserved) |
| 15 | GPIO6/SPI_CLK | VDDIO2V5 | DI/DO | Default for SPI clock (Reserved) |
| 16 | GPIO7/SPI_MOSI | VDDIO2V5 | DI/DO | Default for SPI MOSI (Reserved) |
| 17 | GPIO8/SPI_MISO | VDDIO2V5 | DI/DO | Default for SPI MISO (Reserved) |
| 19 | GPIO12/CH9434_INT | VDDIO2V5 | DI/DO | Default for CH9434 interrupt (Reserved) |
| 25 | GPIO0/BT_ACTIVE | VDDIO2V5 | DI/DO | Default for PTA coexistence I/O, can be used as JTAG_TCK (Reserved) |
| 30 | GPIO1/BT_PRIORITY | VDDIO2V5 | DI/DO | Default for PTA coexistence I/O, can be used as JTAG_TDI (Reserved) |
| 28 | GPIO2/WLAN_ACTIVE | VDDIO2V5 | DI/DO | Default for PTA coexistence I/O, can be used as JTAG_TDO (Reserved) |
| 24 | GPIO3/BT_RESET_L | VDDIO2V5 | DI/DO | Default for BT reset control I/O, can be used as JTAG_TMS (Reserved) |
| 29 | GPIO4 | VDDIO2V5 | DI/DO | Bootstrap GPIO, with pull down resistor.do not pull up, Software Configured |
| 1 | GPIO10/UART_TXD | VDDIO2V5 | DI/DO | Bootstrap GPIO, with pull down resistor. Default for QCA4531 debug, UART transmit serial data |
| 2 | GPIO9/UART_RXD | VDDIO2V5 | DI/DO | Default for QCA4531 debug, UART receiving serial data |
| 18 | GPIO13 | VDDIO2V5 | DI/DO | Software Configured |

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|------------------|----------|----------------|---|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |
| 21 | GPIO15 | VDDIO2V5 | DI/DO | Bootstrap GPIO, with pull down resistor, Software Configured | |
| 22 | GPIO16/I2C_SCL | VDDIO2V5 | DI/DO | Bootstrap GPIO, with pull up resistor, Software Configured | |
| 23 | GPIO17/I2C_SDA | VDDIO2V5 | OD | Software Configured | |
| 46 | SWD_CLK | VDD3V3 | DI/DO | Serial Wire Debug for BT | |
| 47 | SWD_DIO | VDD3V3 | DI | Serial Wire Debug for BT | |
| 48 | BT_TEST_IF | VDD3V3 | DI/DO | IF test for BT | |
| 49 | SWO | VDD3V3 | DI/DO | Serial Wire Debug for BT | |
| 50 | BT_TEST_HF | VDD3V3 | DO | HF test for BT | |
| 54 | P4_TX+ | AVDD20 | AO | Current mode PHY, Port 4 transmit pair needs AVDD20 power supply for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching | |
| 55 | P4_TX- | AVDD20 | AO | | |
| 56 | P4_RX+ | AVDD20 | AI | Current mode PHY, Port 4 receive pair needs AVDD20 power supply for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching | |
| 57 | P4_RX- | AVDD20 | AI | | |
| 58 | P3_TX+ | AVDD20 | AO | Current mode PHY, Port 3 transmit pair needs AVDD20 power supply for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching | |
| 59 | P3_TX- | AVDD20 | AO | | |
| 60 | P3_RX+ | AVDD20 | AI | Current mode PHY, Port 3 receive pair needs AVDD20 power supply for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching | |
| 61 | P3_RX- | AVDD20 | AI | | |
| 62 | P2_TX+ | AVDD20 | AO | Current mode PHY, Port 2 transmit pair needs AVDD20 power supply for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching | |
| 63 | P2_TX- | AVDD20 | AO | | |
| 64 | P2_RX+ | AVDD20 | AI | Current mode PHY, Port 2 receive pair needs AVDD20 power supply for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching | |
| 65 | P2_RX- | AVDD20 | AI | | |
| 66 | P1_TX+ | AVDD20 | AO | Current mode PHY, Port 1 transmit pair needs AVDD20 power supply | |
| 67 | P1_TX- | AVDD20 | AO | | |

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|------------------|----------|----------------|---|--|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |
| | | | | | for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching |
| 68 | P1_RX+ | AVDD20 | AI | Current mode PHY, Port 1 receive pair needs AVDD20 power supply for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching | |
| 69 | P1_RX- | AVDD20 | AI | | |
| 70 | P0_TX+ | AVDD20 | AO | Current mode PHY, Port 0 transmit pair needs AVDD20 power supply for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching | |
| 71 | P0_TX- | AVDD20 | AO | | |
| 72 | P0_RX+ | AVDD20 | AI | Current mode PHY, Port 0 receive pair needs AVDD20 power supply for transformer side and two 49.9 Ω plus 0.1uF for differential signal impedance matching | |
| 73 | P0_RX- | AVDD20 | AI | | |
| 75 | USB_DP | - | AI/AO | USB D+ signal | |
| 76 | USB_DM | - | AI/AO | USB D- signal | |
| 79 | UART_TXD0 | VDD3V3 | DO | Serial data output of UART0 | |
| 80 | UART_RXD0 | VDD3V3 | DI | Serial data input of UART0 | |
| 81 | UART_CTS0 | VDD3V3 | DI | UART0 input signal ,clear to send, low active valid | |
| 82 | UART_RTS0 | VDD3V3 | DO | UART0 output signal, request to send, low level valid | |
| 100 | UART_TXD1 | VDD3V3 | DO | Serial data output of UART1 | |
| 101 | UART_RXD1 | VDD3V3 | DI | Serial data input of UART1 | |
| 102 | UART_CTS1 | VDD3V3 | DI | UART1 input signal ,clear to send, low active valid | |
| 103 | UART_RTS1 | VDD3V3 | DO | UART1 output signal, request to send, low level valid | |
| 83 | UART_TXD2 | VDD3V3 | DO | Serial data output of UART2 | |
| 84 | UART_RXD2 | VDD3V3 | DI | Serial data input of UART2 | |
| 85 | UART_CTS2 | VDD3V3 | DI | UART2 input signal ,clear to send, low active valid | |
| 86 | UART_RTS2 | VDD3V3 | DO | UART2 output signal, request to send, low level valid | |
| 89 | PCIE_TX_N | - | AO | Differential transmit; use 0.1uF capacitors on each signal line. can be left open if not used | |
| 90 | PCIE_TX_P | - | AO | | |
| 92 | PCIE_RX_P | - | AI | | |

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|--------------------------------|------------------|----------|----------------|---|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |
| 93 | PCIE_RX_N | - | AI | Differential receive, can be left open if not use | |
| 95 | PCIE0_RST_L | VDD3V3 | PU | PCI Express reset, open drain, Internal pulled up to 3.3V through 1 K Ω resistor, can be left open if not used | |
| 96 | PCIE_CK_OUT_N | - | AO | Differential reference clock (100 MHz), can be left open if not used | |
| 97 | PCIE_CK_OUT_P | - | AO | | |
| 99 | CHIP_RSTN_IN | VDD3V3 | DI | External power on reset with weak pulls up. This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the input must be driven with 3.3 V logic | |
| 3~9, 33~37, 40~43, 52 | - | - | NC | Not connect | |

2.3. Computing Subsystem

2.3.1. SoC

CQM4531-L-224-2 contains both Qualcomm QCA4531 and QCC711 chipsets.

The QCA4531 is a highly integrated and feature-rich IEEE 802.11n 2x2 2.4 GHz System-on-a-Chip (SoC). It includes one MIPS 24Kc processor, one PCI Express 1.1 Root Complex interface, five port IEEE 802.3 Fast Ethernet Switch with MAC/PHY, one USB 2.0 MAC/PHY, and external memory interface for serial Flash, DDR1 or DDR2, UART, and GPIOs that can be used for LED controls or other general purpose interface configurations.

The QCA4531 PCIe root complex interface can be used to connect to an endpoint such as the Qualcomm Atheros single-chip MAC/BB/radio for WLAN applications. The QCA4531 supports 802.11n operations up to 144 Mbps at 20 MHz bandwidth and 300 Mbps at 40 MHz bandwidth. Additional features include

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|------------------|----------|----------------|---------|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

Maximal Likelihood (ML) decoding, Low-Density Parity Check (LDPC) and Maximal Ratio Combining (MRC).

The QCA4531 supports booting from NOR flash.

The QCC711 provides Bluetooth functionality and integrates three cores– Arm Cortex-M3 processor, Arm Cortex-M0 processor, and RISC-V:

Arm Cortex-M3 processor – Running at 32MHz, dedicated to higher layer protocol and user applications. It conducts inter-processor communication with other two cores.

Arm Cortex-M0 processor – Running at 32MHz, dedicated to BLE radio and lower protocol layer (MAC) processing.

The RISC-V processor runs at 32MHz and is specifically dedicated to security services. It can serve as a Root-of-Trust (RoT) processor, executing highly secure boot-up code within a Trusted Execution Environment (TEE) to validate the user application image before transferring control to the Arm Cortex-M3 processor. The RISC-V processor possesses its own 32KB SRAM, 192KB ROM, and a protected OTP area that is not visible to user applications, ensuring high reliability and security.

2.4. Memory

CQM4531-L-224-2 supports 1Gbit DDR2, 1Gbit NAND SPI flash, 4Mbit NOR flash. NOR flash includes Boot loader and ART data. NAND flash includes OS and profiles.

2.5. Peripheral Interfaces

CQM4531-L-224-2 supports the following peripheral interfaces:

- 1 x PCIe
- 3 x UART
- 3 x USB 2.0
- 8 x GPIOs

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|------------------|----------|----------------|---------|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

- 2 x SPI
- 5 x Fast Ethernet
- 2 x K.FL2(Wi-Fi)
- 1 x K.FL2(Bluetooth)

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

3 Electrical Characteristics

3.1. Absolute Maximum Ratings

The absolute maximum ratings provided in this section reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating.

| Pin | Parameter | Max Rating | Unit |
|---------------------|--------------------|-------------|------|
| VDD33 | Supply Voltage | -0.3 to 3.6 | V |
| VDDIO2V5 | I/O Supply Voltage | -0.3 to 3.0 | V |
| All ground pads | --- | 0 | V |
| Storage temperature | --- | 85 | °C |

3.2. Recommended Operating Conditions

| Pin | Parameter | Min | Typical | Max | Unit |
|-----------------------|--------------------------|------|---------|---------------|------|
| VDD33 | Supply Voltage | 3.14 | 3.3 | 3.47 | V |
| VDDIO2V5 | I/O Supply Voltage | 2.49 | 2.62 | 2.75 | V |
| AVDD20 | Voltage for Ethernet PHY | 1.9 | 2.0 | VDDIO2V5-0.22 | V |
| All ground pads | --- | 0 | 0 | 0 | V |
| Operating temperature | | -40 | - | 85 | °C |
| Storage temperature | --- | -40 | --- | 85 | °C |

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

4 Radio Performance

4.1. 2.4GHz Wi-Fi

Tx Power for 2.4GHz Operation

| Parameter | Typical(dBm) |
|-------------|--------------|
| 1 Mbps | 18 |
| 6 Mbps | 17 |
| HT20, MCS0 | 16 |
| HT40, MCS0 | 15 |
| 54 Mbps | 13 |
| HT20, MCS15 | 11 |
| HT40, MCS15 | 10 |

Sensitivity for 2.4GHz Operation

| Parameter | Min ¹ (dBm) | Typical(dBm) |
|----------------------------------|------------------------|--------------|
| CCK, 1 Mbps | — | -95 |
| CCK 11 Mbps | -76 | -86 |
| OFDM, 6 Mbps | -82 | -89 |
| OFDM, 54 Mbps | -65 | -76 |
| HT20, MCS0, 1 stream, 2 Tx, 2 Rx | -82 | -88 |
| HT20, MCS7, 1 stream, 2 Tx, 2 Rx | -64 | -73 |
| HT20, MCS8, 2 stream, 2 Tx, 2 Rx | -82 | -88 |
| HT20, MCS15, 2 stream 2 Tx, 2 Rx | -64 | -69 |
| HT40, MCS0, 1 stream, 2 Tx, 2 Rx | -79 | -79 |
| HT40, MCS7, 1 stream, 2 Tx, 2 Rx | -61 | -71 |
| HT40, MCS8, 2 stream, 2 Tx, 2 Rx | -79 | -87 |
| HT40, MCS15, 2 stream 2 Tx, 2 Rx | -61 | -67 |

1. Minimum values based on IEEE 802.11 specifications.

4.2. Bluetooth

Sensitivity for Bluetooth Operation

| Channel Bandwidth | Modulation | Parameter | Data Rate | Typical(dBm) |
|-------------------|------------|---|-----------|--------------|
| 2MHz | GFSK | Rx Sensitivity @ 30.8% PER (Boost Mode) | 2Mbps | -93 |
| | | | 1Mbps | -96 |
| | | | 500kbps | -98 |

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|------------------|----------|----------------|---------|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |
| | | | | 125kbps | -103 |
| Note: VDD_VBAT = 3.3V | | | | | |

Tx Power for Bluetooth Operation

| Channel Bandwidth | Modulation | Data Rate | Typical(dBm) |
|-----------------------|------------|-----------|--------------|
| 2MHz | GFSK | 2Mbps | +6 |
| | | 1Mbps | +6 |
| | | 500kbps | +6 |
| | | 125kbps | +6 |
| Note: VDD_VBAT = 3.3V | | | |

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

5 Power Consumption

Power Consumption of 2.4 GHz Operation (internal PA) with VDD = 3.3 V

| Operating Mode ^{1 2} | Parameter | Tx Power | Average |
|---|-------------|----------|---------|
| Wi-Fi mode: TX (two-chain) Rx (Two-chain) | HT40, MCS15 | 10dBm | 680 mA |

- Internal 2.4 GHz radio, internal PA, PCIE RC interface, USB and internal switch are all in maximum data transfer condition and the CPU is working on maximum utilization.
- Without Bluetooth.

Power Consumption for Bluetooth with VDD = 3.3 V

| Channel Bandwidth | Modulation | Parameter | dBm | Average |
|-------------------|------------|----------------|-----|---------|
| 2MHz | GFSK | Tx Power | 0 | 10.5 mA |
| | | | +4 | 14.6 mA |
| | | | +6 | 16.6 mA |
| | | Rx Power Boost | -95 | 5.3 mA |

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

6 Mechanical Specification

6.1. Dimension

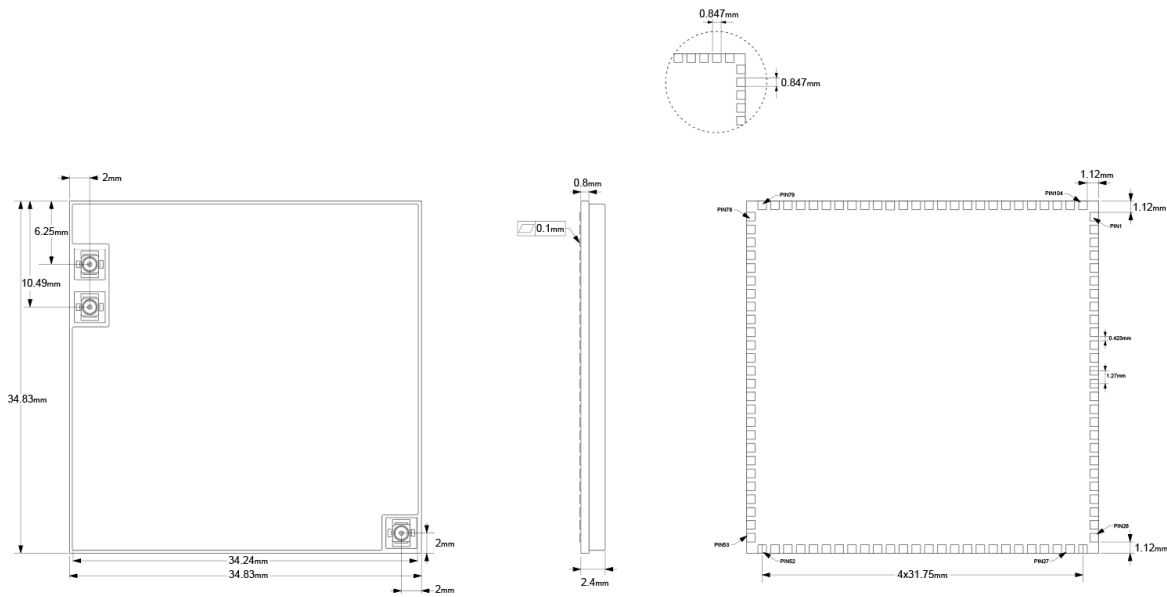


Figure 5: CQM4531-L-224-2 Dimension

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|------------------|----------|----------------|---------|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

6.2. Recommended PCB Landing Pattern

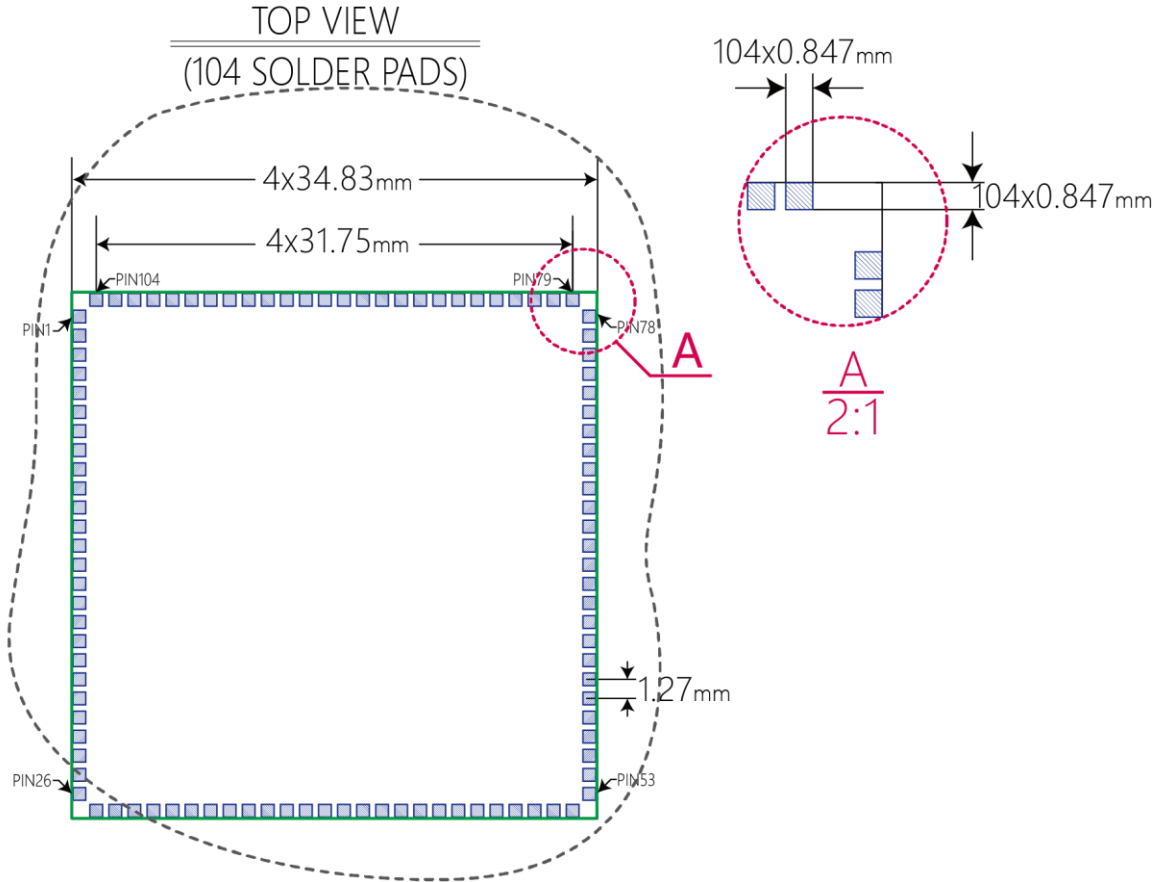


Figure 6: CQM4531-L-224-2 PCB Landing Pattern

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

7 Manufacturing Recommendation

7.1. Power Layout Guideline

The CQM4531-L-224-2 is powered by VDD3.3. Connect the power pin with a capacitor as close as possible to the chip and pin. Decouple the power supply from the chip using a capacitor. Utilize capacitors to prevent noise from coupling back to the power plane.

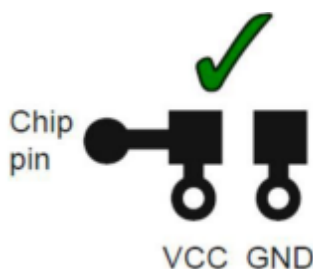


Figure 7: Power Layout Guideline

7.2. PCIe Layout Guideline

| Category | Guidelines/remarks |
|---------------------------|--|
| Groups | PCIE_TX_P&N,PCIE_RX_P&N,PCIE_CK_OUT_P&N |
| Route type | Differential pair, 100 Ω impedance |
| Return path | Ensure continuous and unbroken return path without voids. |
| Length | < 10 cm preferred |
| Length match within pair | 2ps |
| Length match across pairs | No strict requirements to length match the Tx, Rx, CLK pairs. Keep them within 10 ps |
| Spacing requirements | 3H spacing between pairs |
| GND shielding | Provide GND shield at 3H spacing away from the signal pairs. Stitch the GND shape to the main GND in inner layers with vias at regular intervals of 0.25 cm. |
| Vias/layer transitions | For PCIe2.0, avoid layer transitions where possible; provide adequate GND return vias if taking via on the signal path. |
| AC coupling | Use 0.1 uF capacitors on each signal line of the Tx pair from the EVB Board and place them symmetrically at the same point on the pair. |
| If unused | The outputs should be NC: float the input pins. |

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

7.3. Ethernet Layout Guideline

| Category | Guidelines/remarks |
|---------------------------|--|
| Groups | P0~P4_TX±,P0~P4_RX± |
| MDI termination | 10/100M Ethernet PHY supports CML driver mode by design, hence it is must requirement to use two 49.9Ω and one 0.1uF capacitor termination for each MDI signal pairs between P and N lines, and 1.8V or 2.0V power supply for transformer center tap |
| Route type | Differential pair, 100Ω impedance |
| Return path | Ensure continuous and unbroken return path without voids. |
| Length | < 10 cm preferred |
| Length match within pair | 5ps |
| Length match across pairs | No strict requirements to length match the Tx and Rx pairs. Keep them within 100 ps. |
| Spacing requirements | 3H spacing between other signals |
| GND shielding | Provide GND shield at 3H spacing away from the signal pairs. Stitch the GND shape to the main GND in inner layers with vias at regular intervals of 1cm. |
| Vias/layer transitions | Avoid layer transitions where possible; provide adequate GND return vias if taking via on the signal path. |
| AC coupling | Not applicable |
| If unused | The outputs should be NC: float the input pins. |

7.4. USB Layout Guideline

| Category | Guidelines/remarks |
|---------------------------|--|
| Groups | USB_DP3&DM3,USB_DP4&DM4,MOUDULE_USB_DP2&DM2 |
| Route type | Differential pair, 90Ω impedance for the USB2.0 pair |
| Return path | Ensure continuous and unbroken return path without voids. |
| Length | < 10 cm preferred |
| Length match within pair | 3ps |
| Length match across pairs | Not applicable |
| Spacing requirements | 3H spacing between other signals |
| GND shielding | Provide GND shield at 3H spacing away from the signal pairs. Stitch the GND shape to the main GND in inner layers with vias at regular intervals of 1cm. |

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|--|----------|----------------|---------|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |
| Vias/layer transitions | Avoid layer transitions where possible; provide adequate GND return vias if taking via on the signal path. | | | | |
| AC coupling | Not applicable | | | | |
| If unused | The outputs should be NC: float the input pins. | | | | |

7.5. Soldering Recommendations

CQM4531-L-224-2 can be SMT on the board, following the temperature curve graph:

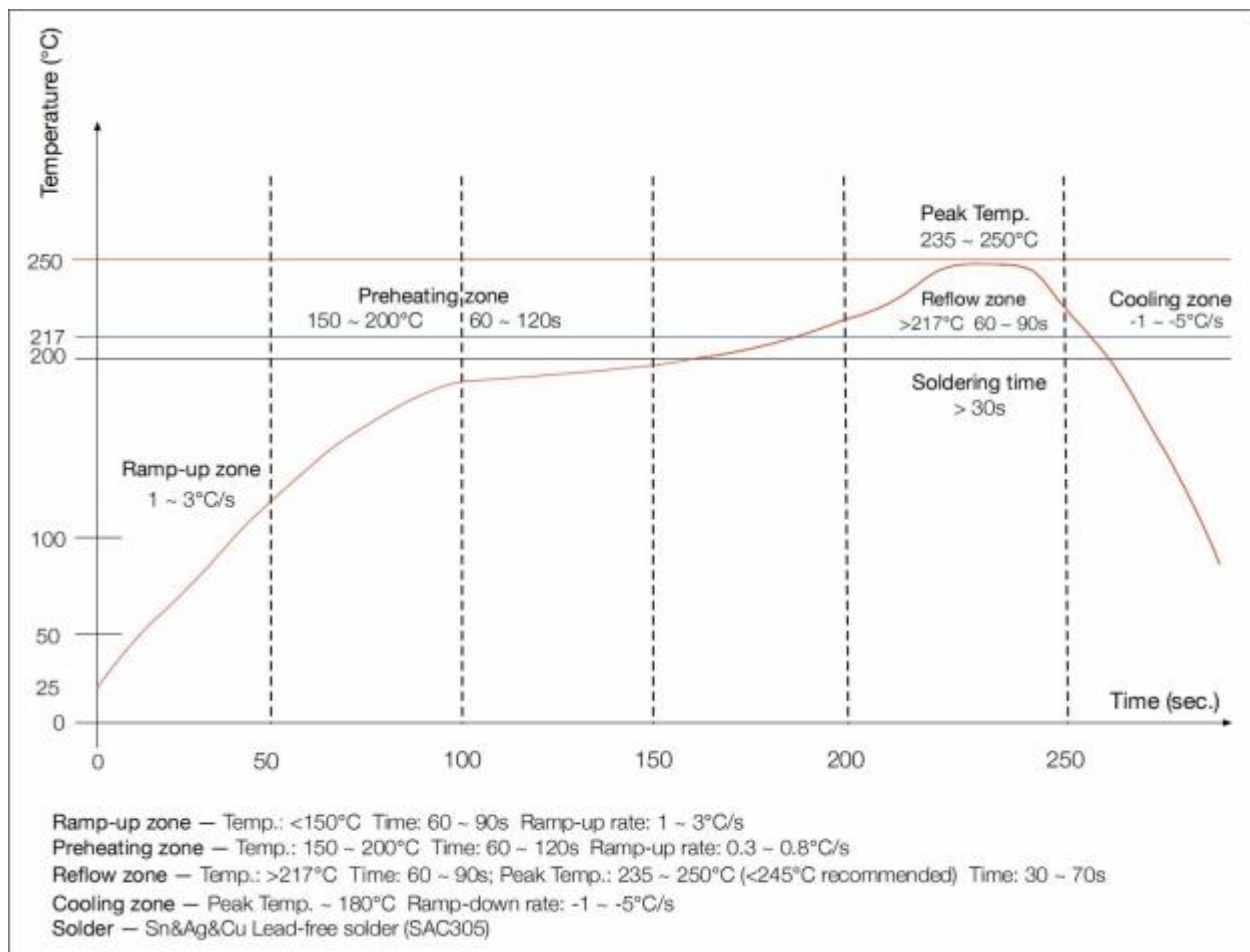


Figure 8: Soldering Guideline

| | | | | | |
|---------------------------|------------------|----------|----------------|---------|--------------|
| Documentation Title | Documentation No | Revision | Classification | Status | Date |
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

Revision History

| Revision | Description | Date |
|----------|--|-------------|
| 0.1 | Initial draft | Feb 20,2024 |
| 0.2 | Adjust pin definition and optimize layout | Sep 22,2024 |
| 0.3 | Update model name | Sep 27,2024 |
| 0.4 | Add Operating temperature | Jan 21,2025 |
| 0.5 | Thickness updated from 2.2mm to 2.4mm | Mar 7,2025 |
| 0.6 | Updating the logo of Figure 1 and Figure 2 | Mar 31,2025 |

| Documentation Title | Documentation No | Revision | Classification | Status | Date |
|---------------------------|------------------|----------|----------------|---------|--------------|
| CQM4531-L-224-2 Datasheet | | V0.6 | Public | Release | Mar 31, 2025 |

Disclaimer and Copyright Notice

Information in this document, including URL references, is subject to change without notice.

THIS DOCUMENT IS PROVIDED AS IS WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE.

All liability, including liability for infringement of any proprietary rights, relating to the use of information in this document, is disclaimed. No licenses express or implied, by estoppel or otherwise, to any intellectual property rights are granted herein.

Copyright©2025 Creatcomm. All rights reserved.