Datasheet

MQC 206x Series Module

Catalog

1 Product Overview

The MQC206x is a highly integrated module supporting 802.11ax Wi-Fi and Bluetooth (BT). The MQC2064-0-46-0U supports simultaneous operation on 2.4GHz and 5GHz. The MQC2066-0-46-0U supports simultaneous operation on 2.4GHz and 5GHz (or 6GHz). The wireless module complies with IEEE 802.11 a/b/g/n/ac/ax 2x2 MIMO standard and it can achieve up to a speed of 2975.6Mbps (2.4GHz 2x2 40MHz 11ax + 5/6GHz 2x2 160MHz 11ax DBS). The integrated module provides PCIe interface for Wi-Fi, UART/PCM or USB interface for Bluetooth.

Key Features:

Module	MQC2064-0-46-0U	MQC2066-0-46-0U
Chipset	QCA2064	QCA2066
Interfaces	WLAN: PCIe BT: UART/PCM or USB	
WLAN Speciation	2 spatial data stream system (2T2R) 5GHz: Support 20/40/80/160MHz bandwidth mode 2.4GHz: Support 20/40MHz bandwidth mode	2 spatial data stream system (2T2R) 5GHz/6GHz: Support 20/40/80/160MHz bandwidth mode 2.4GHz: Support 20/40MHz bandwidth mode
BT Speciation	BT5.2	
Antenna Connector	K.FL2 Antenna x 2	
Operating Voltage	3.3 V ± 5%	
Operating Environment	Temperature: -30 ~ 65 ℃ Humidity: +5 ~ 85% RH (No Condensation)	
Storage Environment	Temperature: -40 ~ 125 ℃ Humidity: +5 ~ 60% RH (No Condensation)	
Dimensions	22 x 30 x3.1 mm M.2 Type 2230 Key E	

The MQC206X module is graphically illustrated below:

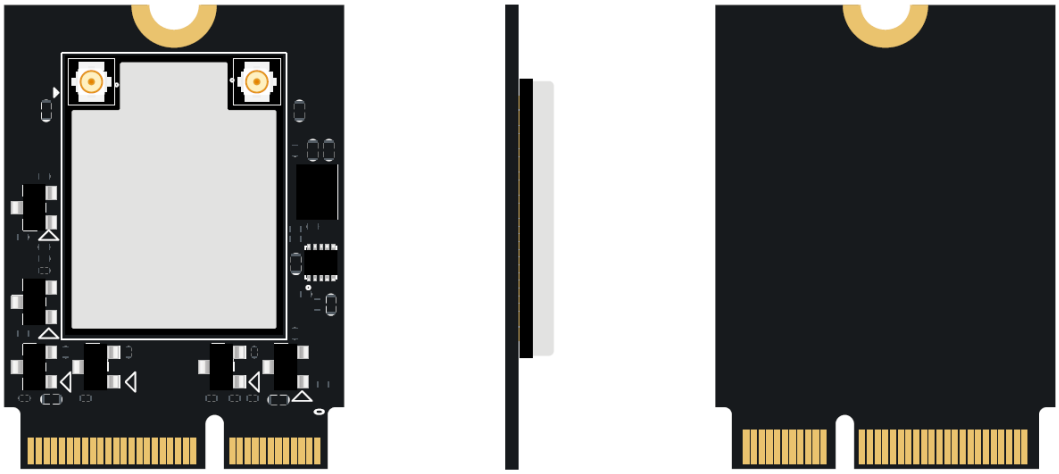

Figure 1: MQC206X Module View

2 Hardware Specification

2.1. Block Diagram

The block diagram of the module is shown below.

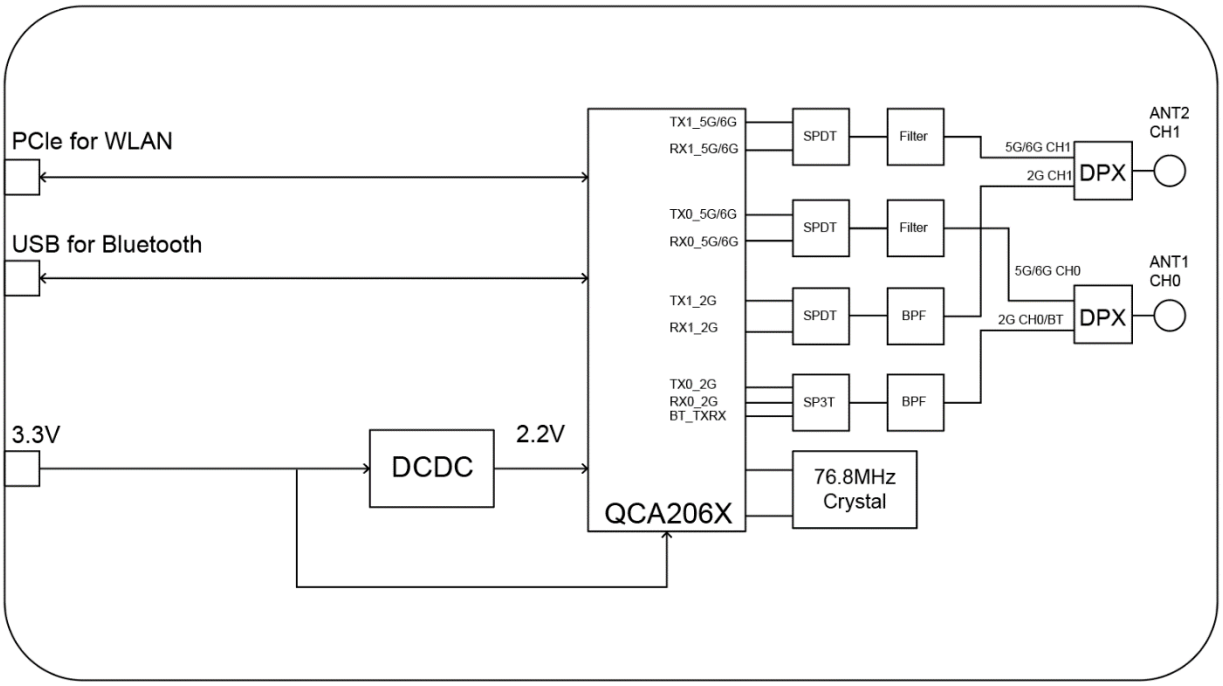

Figure 2: MQC206X Block Diagram

2.2. Pinout Description

2.2.1. Pin Map

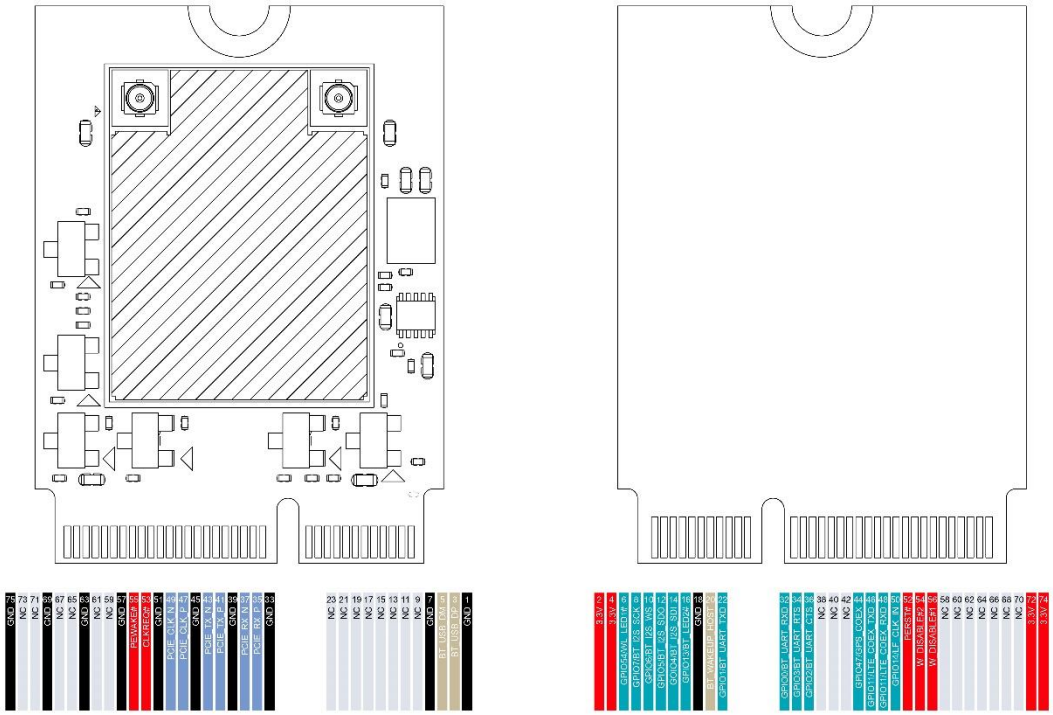

Figure 3: MQC206X Pin Map

2.2.2. Pin Definition

Pin	Pin Name	VDDIO or pad voltage	Type	Description
2,4,72,74	VDD_3V3	3.3V	-	Power input (typical 3.3V)
3	BT_USB_DP	-	AI/AO	USB1.1 interface to support full-speed only (no low-speed mode) and peripheral device mode only (no master mode).1.5KΩ pull up to D+ is integrated in the device. No external resistor is required. Ensure that host has 15KΩ pull down resistor on both D+ and D- according to USB1.1 specification.
5	BT_USB_DM	-	AI/AO	Same as PIN3
6	GPIO54/WL_LED 1#	1.8V	PD	WLAN LED indicator signal, active low.

16	GPIO13/BT_LED2#	1.8V	NP	Bluetooth LED indicator signal, active low.
8	GPIO7/BT_I2S_SCK	1.8V	NP, SLIMbus	Bluetooth four-wire I2S interface operated in slave mode. The clock rate up to 2.048MHz. If SLIMbus mode is configured, it is used with Qualcomm mobile host platform only, it operates as slave mode up to 24.xMHz. In PCM mode, it operates at 16-bit mono with either 8 KHz or 16KHz. In Split mode of packet data, supports A2DP, dual eSCO, dual A2DP, up to APTx HD and LDAC. Codecs offloaded to LPASS.
10	GPIO6/BT_I2S_WS	1.8V	PD	Same as PIN8
12	GPIO5/BT_I2S_SDO	1.8V	PU	Same as PIN8
14	GOIO4/BT_I2S_SDI	1.8V	NP, SLIMbus	Same as PIN8
20	BT_WAKEUP_HOST	3.3V	DO	UART sideband used to Wake up Platform
22	GPIO1/BT_UART_TXD	1.8V	PD	Bluetooth UART asynchronous interface. The baud rate is 115.2 k as default and can be configured up to 3.125 Mbps. Customer can choose either four-wire BT_UART or 2-wire BT_USB to interface with the host.
32	GPIO0/BT_UART_RXD	1.8V	PU	Same as PIN22
34	GPIO3/BT_UART_RTS	1.8V	PU	Same as PIN22
36	GPIO2/BT_UART_CTS	1.8V	PD	Same as PIN22
35	PCIE_RX_P	-	AI	WLAN PCIe receive input differential signals
37	PCIE_RX_N	-	AI	WLAN PCIe receive input differential signals

41	PCIE_TX_P	-	AO	WLAN PCIe transmit output differential signals
43	PCIE_TX_N	-	AO	WLAN PCIe transmit output differential signals
44	GPIO47/GPS_COEX	1.8V	PD	This is an active high signal driving from WLAN CPU to indicate that Wi-Fi is transmitting. This signal is for third-party GPS only.
46	GPIO11/LTE_COEX_TXD	1.8V	PD	WSI interface for LTE co-existing interface with LTE modem to enable firmware communication.
48	GPIO10/LTE_COEX_RXD	1.8V	NP	Same as PIN
47	PCIE_CLK_P	-	AI	WLAN PCIe reference clock input differential signals
49	PCIE_CLK_N	-	AI	WLAN PCIe reference clock input differential signals
50	GPIO14/LF_CLK_IN	3.3V	NP	An external 32.768 KHz sleep clock input pin. The PCB design can use either external sleep clock (32.768KHz) or internal sleep clock (32KHz), but external sleep clock provides better sleep clock accuracy. A pull-down resistor is required if LF_CLK_IN is not used.
52	PCIE_PERST#	3.3V	DI	WLAN PCIe reset with weak pull-down
53	PCIE_CLKREQ#	3.3V	DI/DO	An input signal from other peripherals to request system clock output from CLK_OUT (pin AA9). Use in the share crystal or TCXO system that XTAL is attached with this device.
55	PCIE_PEWAKE#	3.3V	DO	WLAN PCIe Request to service a function- initiated wake event.
56	W_DISABLE#1	3.3V	DI	Turn off WLAN RF analog and front-end, Active low.
54	W_DISABLE#2	3.3V	DI	Bluetooth enable/disable signal, active high to enable Bluetooth operation.

1,7,18,33,39,45,51,57,63,69,75	GND	-	GND	Ground
9,11,13,15,17,19,21,23,24,25,26,27,28,29,30,31,38,40,42,58,59,60,61,62,64,65,66,67,68,70,71,73	NC	-	-	Not connect

I/O description (pad type) parameters

AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
DI	Digital input signal (CMOS)
DO	Digital output signal (CMOS)
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
NP	Contains no internal pull

3 Electrical Characteristics

3.1. Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD33	3.3V supply	3.2	3.3	3.45	V
Operation temperature	-	-30	-	65	°C
Storage temperature	-	-40	-	125	°C

4 Radio Performance

4.1. 2.4GHz Wi-Fi

Tx power of 2.4GHz Operation (±2dBm)

Parameter	Typical (dBm)
54 Mbps	16.4
HE20, MCS11	14.0
HE40, MCS11	13

Receiving sensitivity of 2.4GHz Operation (±2dBm)

Parameter	Typical (dBm)
54 Mbps	-73
HE20, MCS11	-58
HE40, MCS11	-55

4.2. 5GHz Wi-Fi

Tx power of 5GHz Operation (±2dBm)

Parameter	Typical (dBm)
54 Mbps	17
HE20, MCS11	13
HE80, MCS11	13
HE160, MCS11	12.5

Receiving sensitivity of 5GHz Operation (±2dBm)

Parameter	Typical (dBm)
54 Mbps	-73
HE20, MCS11	-59
HE80, MCS11	-54
HE160, MCS11	-51

4.3. 6GHz Wi-Fi (MQC2066-0-46-0U support)

Tx power of 6GHz Operation (±2dBm)

Parameter	Typical (dBm)
54 Mbps	13.5
HE80, MCS11	11

HE160, MCS11	10.5

Receiving sensitivity of 6GHz Operation (±2dBm)

Parameter	Typical (dBm)
54 Mbps	-73
HE80, MCS11	-54
HE160, MCS11	-38

4.4. Bluetooth

Channel Bandwidth	Modulation	Parameter	Data Rate	Typical (dBm)
2MHz	GFSK	Rx Sensitivity @ 30.8% PER (Boost Mode)	2Mbps	-93
			1Mbps	-96
Note: VDD_VBAT = 3 .3V				

5 Power Consumption

Description	Typ. Value (mA)	Max. Value (mA)
TX (2.4G HE40)	400	531
RX (2.4G HE40)	220	290
TX (5G HE160)	1050	1130
RX (5G HE160)	290	410
TX (6G HE160)	1110	1170
RX (6G HE160)	300	370
BT TX（1M@7dBm）	137	147
BT RX	116	136

Note: Use QRCT tool, TX mode: CONT TX99, TX Power Control: AutoPower, test the maximum current of the module 3.3V power supply when NSS=1.

6 Mechanical Specification

6.1. Dimension

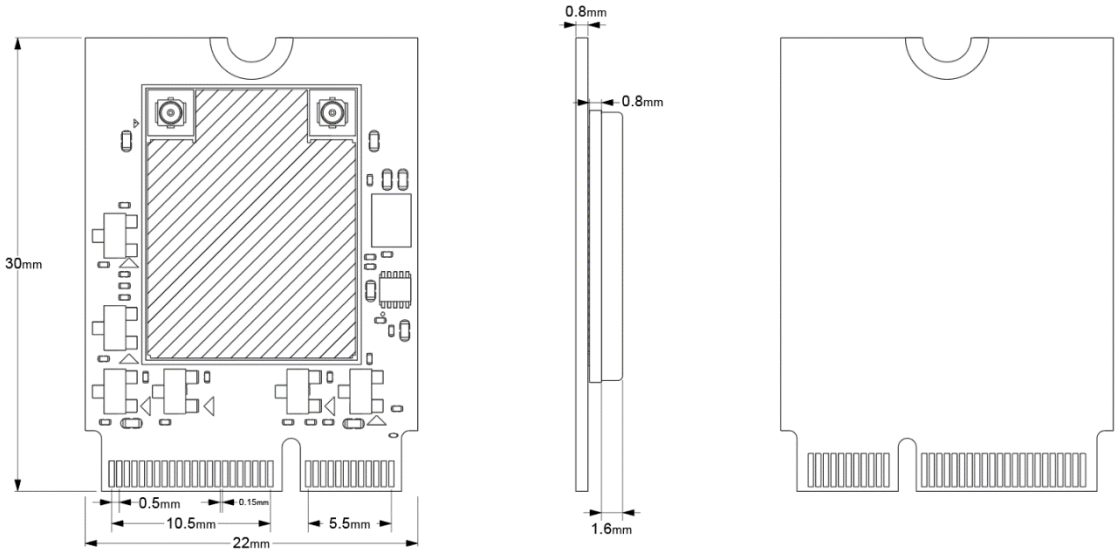

Figure 4: MQC206X Dimension

7 Manufacturing Recommendation

7.1. Power Layout Guideline

The MQC206X is powered by VDD3.3. Connect the power pin with a capacitor as close as possible to the chip and pin. Decouple the power supply from the chip using a capacitor. Utilize capacitors to prevent noise from coupling back to the power plane.

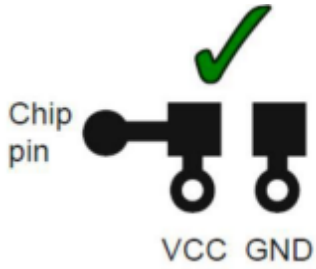

Figure 5: Power Layout Guideline

7.2. PCIe Layout Guideline

Category	Guidelines/remarks
Groups	PCIE_TX_P&N,PCIE_RX_P&N,PCIE_CK_OUT_P&N

Route type	Differential pair, 100 Ω impedance
Return path	Ensure continuous and unbroken return path without voids.
Length	< 10 cm preferred
Length match within pair	2ps
Length match across pairs	No strict requirements to length match the Tx、Rx、CLK pairs. Keep them within 10 ps
Spacing requirements	3H spacing between pairs
GND shielding	Provide GND shield at 3H spacing away from the signal pairs. Stitch the GND shape to the main GND in inner layers with vias at regular intervals of 0.25 cm.
Vias/layer transitions	For PCIe2.0, avoid layer transitions where possible; provide adequate GND return vias if taking via on the signal path.
AC coupling	Use 0.1 uF capacitors on each signal line of the Tx pair from the EVB Board and place them symmetrically at the same point on the pair.
lf unused	The outputs should be NC: float the input pins.

7.3. USB Layout Guideline

Category	Guidelines/remarks
Groups	USB_DP3&DM3,USB_DP4&DM4,MOUDULE_USB_DP2&DM2
Route type	Differential pair, 90Ω impedance for the USB2.0 pair
Return path	Ensure continuous and unbroken return path without voids.
Length	< 10 cm preferred
Length match within pair	3ps
Length match across pairs	Not applicable
Spacing requirements	3H spacing between other signals
GND shielding	Provide GND shield at 3H spacing away from the signal pairs. Stitch the GND shape to the main GND in inner layers with vias at regular intervals of 1cm.
Vias/layer transitions	Avoid layer transitions where possible; provide adequate GND return vias if taking via on the signal path.
AC coupling	Not applicable
lf unused	The outputs should be NC: float the input pins.

7.4. Soldering Recommendations

MQC206x can be SMT on the board, following the temperature curve graph:

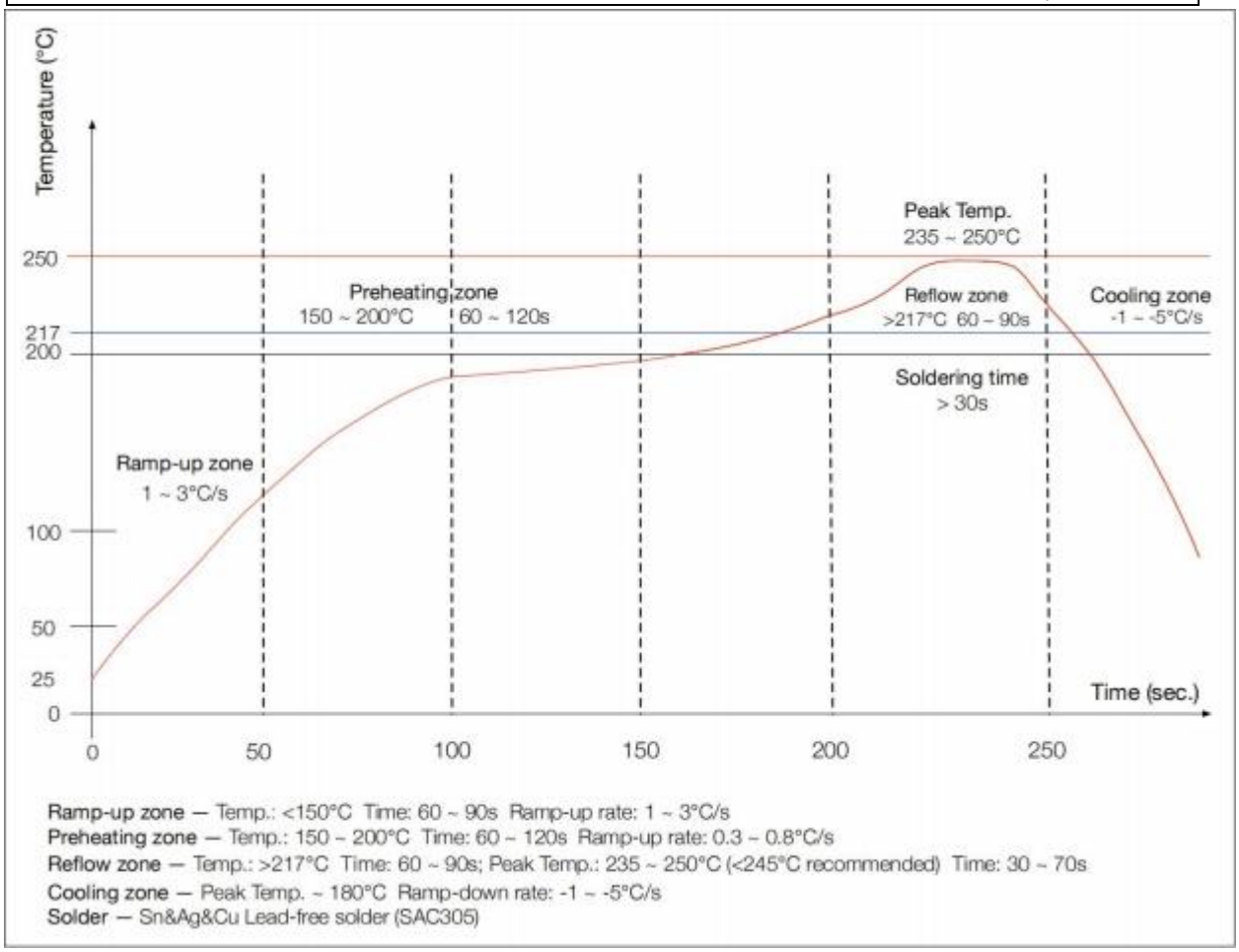

Figure 6: Soldering Guideline

Revision History

Revision	Description	Date
0.1	Initial draft	Apr 2,2025

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